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ORIGINAL

PATENT APPLICATION

ATTORNEY DOCKET NO. 200302133-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Matthew C. MATTINA et al.

Confirmation No.: 3940

Application No.: 09/924,934

Examiner: C. E. Anya

Filing Date: 08/08/2001

Group Art Unit: 2194

Title: MECHANISM FOR HANDLING LOAD LOCK/STORE CONDITIONAL PRIMITIVES IN DIRECTORY-BASED DISTRIBUTED SHARED MEMORY MULTIPROCESSORS

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 10/11/2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $500.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

( ) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit:_____

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(X) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300 on 11/14/2005

Number of pages: 28

Typed Name: Jessica M. Readle

Signature: Jessica M. Readle

Respectfully submitted,

Matthew C. MATTINA et al.

By _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Matthew C. Mattina et al.	§	Confirmation No.:	3940
Serial No.:	09/924,934	§	Group Art Unit:	2194
Filed:	08/08/2001	§	Examiner:	Charles E. Anya
For:	Mechanism For Handling Load Lock/Sore Conditional Primitives In Directory-Based Distributed Shared Memory Multiprocessors	§	Docket No.:	200302133-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: November 14, 2005

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed via facsimile on October 11, 2005.

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I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. HPDC is a wholly owned affiliate of Hewlett-Packard Company (HPC). HPC merged with Compaq Computer Corporation (CCC) which owned Compaq Information Technologies Group, L.P. (CITG). The Assignment from the inventors to CCC was recorded on August 8, 2001, at Reel/Frame 012067/0828. The Assignment from CCC to CITG was recorded on January 15, 2002, at Reel/Frame 012480/0537. The Change of Name document was recorded on May 12, 2004, at Reel/Frame 014628/0103.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

Originally filed claims:	1-34.
Claim cancellations:	None.
Added claims:	None.
Presently pending claims:	1-34.
Presently appealed claims:	1-34.

IV. STATUS OF AMENDMENTS

No claims were amended after the final Office action dated June 10, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 CFR § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

Claim 1 recites a distributed multiprocessing computer system, which includes a plurality of processors each coupled to an associated memory module, wherein each of the associated memory modules may store data that is shared between said processors (Fig. 2; ¶30,ℓ1-9), said system comprising: a Home processor that includes a memory block and a directory for said memory block in the associated memory module (¶26,ℓ11-13); an Owner processor that includes a cache memory, and wherein said Owner processor obtains an exclusive copy of said memory block, and stores said exclusive copy of said memory block in said cache memory (¶26,ℓ13-14); and wherein said Owner processor may displace the exclusive copy of said memory block, and return said displaced copy of said memory block to said Home processor with a signal indicating that said Owner processor remains a sharer of said memory block (¶17,ℓ1-9; ¶36,ℓ1-12).

Claim 4 recites a distributed multiprocessing computer system of a previous claim wherein said Owner processor includes a register in which an address is stored representing the memory block obtained in response to the Load Lock instruction (¶19), and wherein said Owner processor compares the address of any displaced data with the address stored in said register (Fig. 3; ¶40).

Claim 5 recites the distributed multiprocessing computer system of claim 4, wherein the Owner processor asserts a Victim To Shared message if the address of any displaced data matches the address stored in said register(Fig. 3; ¶40,ℓ7-12).

Claim 13 recites a method of maintaining memory coherence in a distributed shared memory computer system including a plurality of processors (Fig. 2; ¶30,ℓ1-9), comprising the acts of: requesting a copy of a memory block from a Home processor to perform a write operation on the copy of the memory block (¶18,ℓ4-6); storing said copy of said memory block exclusively in a cache memory associated with an Owner processor (¶18,ℓ4-7); updating a coherence directory for said memory block in said Home processor to indicate the write operation on the copy of said memory block in said cache memory associated with the Owner processor (¶32); displacing said copy of said memory block from said cache memory prior to completion of operations on said memory block (¶17,ℓ3-7); transmitting a message to said Home processor relinquishing exclusive control of said memory block, while indicating that said Owner processor should still be deemed a sharer of said memory block(¶17,ℓ3-7; ¶36,ℓ3-12).

Claim 16 recites the method of claim 13, wherein the act of updating the coherence directory includes modifying a register to indicate that the Owner processor has an exclusive copy of the memory block (¶33,ℓ1-5).

Claim 18 recites a method of a preceding claim wherein the act of transmitting a message includes assertion of a Victim To Shared message if the address of the displaced memory block matches the address of any memory block for which an exclusive copy resides in the Owner processor (Fig. 3; ¶40,ℓ7-12), and wherein the directory associated with the Home processor indicates that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message (¶36,ℓ8-12).

Claim 24 recites a distributed multiprocessing computer system(Fig. 2; ¶30,ℓ1-9), comprising: a first processor that includes a memory block and a directory associated with said memory block that tracks the status of said memory block(Fig. 2; ¶32,ℓ1-3); a second processor that includes a cache memory, and wherein said second processor is capable of requesting an exclusive copy of said memory block that is stored in said cache memory(¶26,ℓ13-14); and wherein said second processor may displace the exclusive copy of said memory block prior to

completing processing of said memory block (¶17,ℓ1-9), and said second processor transmits a signal to said first processor indicating that said second processor relinquishes exclusive control of said memory block but should remain a sharer of said memory block (¶36,ℓ1-12).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-3, 13-15, and 24-26 stand rejected under 35 USC § 103(a) as being unpatentable over U.S. Pub. No. 2004/0093467 ("Shen") in view of U.S. Pat. No. 6,425,050 ("Beardsley").

2. Claims 4-12, 16-23, and 27-34 stand rejected under 35 USC § 103(a) as being unpatentable over Shen in view of Beardsley and further in view of U.S. Pat. No. 5,937,199 ("Temple").

VII. ARGUMENT

A. Organization of Arguments

The following arguments begin with an overview of the Beardsley reference to facilitate an understanding of the claim-specific arguments. The claims do not stand or fall together. Instead, applicants present separate arguments for various independent and dependent claims. Each of these arguments is separately argued below and presented with separate headings and sub-heading as required by 37 CFR § 41.37(c)(1)(vii) as follows:

B. U.S. Patent No. 6,425,050 ("Beardsley")
C. Claims 1-3
D. Claim 4
E. Claims 5-12
F. Claims 13-15, 24-26
G. Claims 16-17, 20-23, and 27
H. Claims 18-19 and 28-29

B. U.S. Patent No. 6,425,050 ("Beardsley")

Beardsley teaches a system and method for processing read requests to a cached disk drive. (Abstract) In the preferred embodiment illustrated by Fig. 1, a storage controller 8 responds to access requests from a host computer 4 by "staging" (moving tracks from disk 6 into cache 10) and "destaging" (moving

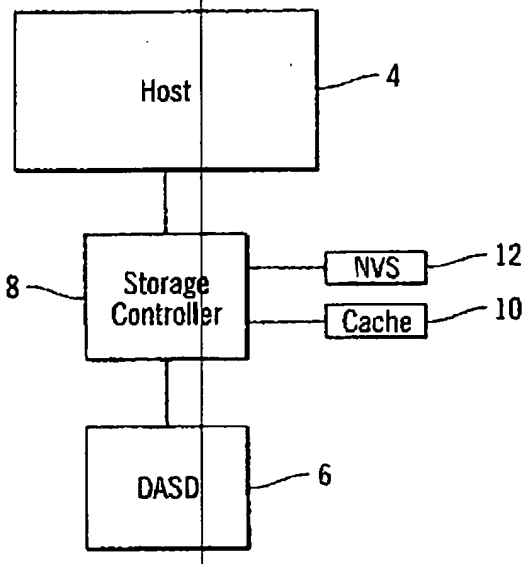

FIG. 1

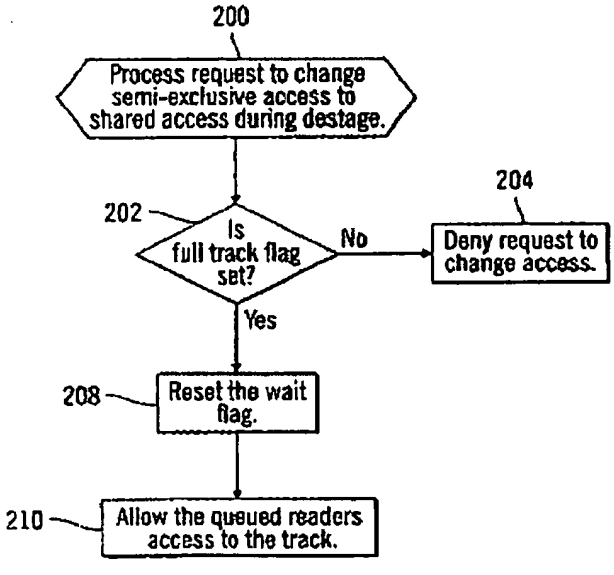

FIG. 4

tracks from cache 10 back to disk 6). (c3,ℓ23-33) Cache 10 is then used as a high speed substitute for disk 6, thereby improving system performance. (c4,ℓ12-37)

Beardsley's teachings particularly concern read operations during the destaging process. (Title; Fig. 3; c5,ℓ42 - c4,ℓ18) Beardsley notes that the destaging process does not interrupt ongoing read operations, and moreover, new read operations may be initiated after the destaging process has been initiated. (c4,ℓ15-21)

Fig. 4 illustrates the logic applied to read requests that are received after a destage operation is initiated. (c6,ℓ18-21) Test 202 enables the read operation only if the full-track flag is set, indicating that the entire disk track is stored in cache 10. (Fig. 4; c6,ℓ25-27; c5,ℓ33-34) Conversely, if the disk track is not present in the cache 10, read operations are suspended until the disk track can be retrieved into the cache. (c6,ℓ34-45)

C. Claims 1-3

Claims 1-3 stand rejected under 35 USC § 103(a) as being unpatentable over U.S. Pub. No. 2004/0093467 ("Shen") in view of U.S. Pat. No. 6,425,050 ("Beardsley"). Appellants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

For example, independent claim 1 recites in part: "wherein said Owner processor may displace the exclusive copy of said memory block, *and return said displaced copy of said memory block to said Home processor with a signal* indicating that said Owner processor remains a sharer of said memory block." The examiner cites Beardsley's teachings of a destaging process in a disk storage controller as anticipating this limitation, particularly citing the "full track flag 22 as an indicator that a new read request can access a track being destaged." (Final OA,¶34,ℓ11-12) However, the full track flag is an internal signal used only by storage controller 8, not a signal returned to a home processor along with a displaced memory block. Moreover, the claimed signal indicates remote availability of a memory block that has been displaced, as contrasted with Beardsley's teachings of data availability only before a track is displaced from

cache, albeit after a destaging operating has commenced. Thus Beardsley, alone or in combination with the other references, fails to disclose a system where the memory block is returned from the cache together with a signal indicating that the sender "remains a sharer" of said memory block. For at least this reason, the rejection of independent claim 1 should be reversed.

Claims 2-3 depend from claim 1 and their rejections should be reversed for at least the same reasons.

D. Claim 4

Claim 4 stands rejected under 35 USC § 103(a) as being unpatentable over Shen in view of Beardsley and further in view of U.S. Pat. No. 5,937,199 ("Temple"). Appellants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

Claim 4 depends from independent claim 1, which is patentable over Shen and Beardsley for the reasons cited above. The examiner does not cite, and appellants cannot find, any teachings in Temple of a signal accompanying a returned copy of a displaced memory block to indicate that the sender remains a sharer of the memory block. For at least this reason, dependent claim 4 is allowable over the cited art.

E. Claims 5-12

Claims 5-12 stand rejected under 35 USC § 103(a) as being unpatentable over Shen in view of Beardsley and Temple. Appellants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

For example, claim 5 depends from claim 4 and is allowable for at least the same reasons. Moreover, claim 5 further recites that "a Victim To Shared message" is generated if the address of the displaced data block matches an address in the Load Lock register. The examiner asserts that the address matching is inherent to Beardsley's teaching of a victim to shared message (full track flag 22). Appellants first maintain that Beardsley provides no such teaching because the full track flag, as its name suggests, merely indicates whether the

cache includes a full track. In contrast, a Victim to Shared message indicates that the status of a data block is "Shared" even though the data block has been displaced, i.e., removed from the cache.

Secondly, appellants note that "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference ... . [It] may not be established by probabilities or possibilities.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Beardsley's full track flag does not require address matching and in fact is probably asserted by hardware based on a data transfer count.

For at least these reasons, the rejections of claim 5 and its dependent claims 6-12 should be reversed.

F. **Claims 13-15, 24-26**

Claims 13-15 and 24-26 stand rejected under 35 USC § 103(a) as being unpatentable over Shen in view of Beardsley. Appellants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

For example, independent claim 13 recites in part: "displacing said copy of said memory block from said cache memory ... [and] transmitting a message to said Home processor relinquishing exclusive control of said memory block, while indicating that said Owner processor should still be deemed a sharer of said memory block." Independent claim 24 recites a similar limitation. The examiner again relies on Beardsley's teachings of a full track flag. However, the full track flag is an internal signal used only by storage controller 8, and it does not suggest a message to a home processor indicating that the sender should be deemed to be holding a shareable copy of the memory block. The claimed message indicates remote availability of a memory block that has been displaced, which may be contrasted with Beardsley's teachings of data availability only *before* a track is displaced from cache, albeit after a destaging operating has commenced. Thus Beardsley, alone or in combination with the other references, fails to disclose transmitting a message indicating that the sender should be deemed a

sharer of the displaced memory block. For at least this reason, the rejection of independent claims 13 and 24 should be reversed.

Claims 14-15 depend from claim 13, and claims 25-26 depend from claim 24. The rejections of these claims should be reversed for at least the same reasons.

G. Claims 16-17, 20-23, 27

Claims 16-17, 20-23, 27, and 30-34 stand rejected under 35 USC § 103(a) as being unpatentable over Shen in view of Beardsley and Temple. Appellants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

Claims 16-17 and 20-23 depend from independent claim 13, which is patentable over Shen and Beardsley for the reasons cited above. The examiner does not cite, and appellants cannot find, any teachings in Temple of a message indicating that the sender should be deemed a sharer of a displaced memory block. For at least this reason, the rejections of dependent claims 16-17 and 20-23 should be reversed.

Claims 27 and 30-34 depend from independent claim 24, which is patentable over Shen and Beardsley for the reasons cited above. The examiner does not cite, and appellants cannot find, any teachings in Temple of a message indicating that the sender should be deemed a sharer of a displaced memory block. For at least this reason, the rejections of dependent claims 27 and 30-34 should be reversed.

H. Claims 18-19, 28-29

Claims 18-19 and 28-29 stand rejected under 35 USC § 103(a) as being unpatentable over Shen in view of Beardsley and Temple. Appellants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

For example, claims 18 and 28 depend from respective claims 17 and 27, and are allowable for at least the same reasons. Moreover, claims 18 and 28 further recite that "a Victim To Shared message" is generated if the address of the displaced data block matches an address in the Load Lock register. The examiner asserts that the address matching is inherent to Beardsley's teaching of a victim to shared message (full track flag 22). Appellants first maintain that Beardsley provides no such teaching because the full track flag, as its name suggests, merely indicates whether the cache includes a full track. In contrast, a Victim to Shared message indicates that the status of a data block is "Shared" even though the data block has been displaced, i.e., removed from the cache.

Secondly, appellants note that "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference ... . [It] may not be established by probabilities or possibilities.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Beardsley's full track flag does not require address matching and in fact is probably asserted by hardware based on a data transfer count.

For at least these reasons, the rejections of claims 18 and 28, along with their dependent claims 19 and 29, should be reversed.

I. Conclusion

For the reasons stated above, appellants respectfully submit that the rejections should be reversed for the reasons given above. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees

required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. (Previously presented) A distributed multiprocessing computer system, which includes a plurality of processors each coupled to an associated memory module, wherein each of the associated memory modules may store data that is shared between said processors, said system comprising:

a Home processor that includes a memory block and a directory for said memory block in the associated memory module;

an Owner processor that includes a cache memory, and wherein said Owner processor obtains an exclusive copy of said memory block, and stores said exclusive copy of said memory block in said cache memory; and

wherein said Owner processor may displace the exclusive copy of said memory block, and return said displaced copy of said memory block to said Home processor with a signal indicating that said Owner processor remains a sharer of said memory block.

2. (Original) The distributed multiprocessing computer system of claim 1, wherein said Owner processor obtains an exclusive copy of said memory block by issuing a Load Lock instruction, and wherein the directory associated with the Home processor indicates that said Owner processor has obtained exclusive control of said memory block.

3. (Original) The distributed multiprocessing computer system of claim 2, wherein said Owner processor is capable of executing multiple threads concurrently, and may displace data associated with a non-executing thread from its associated cache memory.

4. (Original) The distributed multiprocessing computer system of claim 3, wherein said Owner processor includes a register in which an address is stored representing the memory block obtained in response to the Load Lock instruction, and wherein said Owner processor compares the address of any displaced data with the address stored in said register.

5. (Original) The distributed multiprocessing computer system of claim 4, wherein the Owner processor asserts a Victim To Shared message if the address of any displaced data matches the address stored in said register.

6. (Original) The distributed multiprocessing computer system of claim 5, wherein the Owner processor asserts a Victim message if the address of any displaced data does not match the address stored in said register.

7. (Original) The distributed multiprocessing computer system of claim 5, wherein the directory associated with the Home processor indicates that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message.

8. (Original) The distributed multiprocessing computer system of claim 7, wherein said Owner processor subsequently re-obtains an exclusive copy of said memory block to complete execution of the non-executing thread.

9. (Original) The distributed multiprocessing computer system of claim 8, wherein the Owner processor asserts a Read-with-Modify Intent Store Conditional instruction to the Home directory to again request an exclusive copy of said memory block.

10. (Original) The distributed multiprocessing computer system of claim 9, wherein, in response to the Read-with-Modify Intent Store Conditional instruction, the Home directory determines if the Owner processor is a sharer of the memory block, and if so, the Home directory sends an exclusive copy of the memory block to the Owner processor.

11. (Original) The distributed multiprocessing computer system of claim 10, wherein the Home directory invalidates all other sharers when it sends an exclusive copy of the memory block to the Owner processor.

12. (Original) The distributed multiprocessing computer system of claim 9, wherein the Home directory determines if the Owner processor is a sharer of the memory block, and if not, the Home directory sends a Store Conditional Failure message to the Owner processor.

13. (Original) A method of maintaining memory coherence in a distributed shared memory computer system including a plurality of processors, comprising the acts of:

requesting a copy of a memory block from a Home processor to perform a write operation on the copy of the memory block;

storing said copy of said memory block exclusively in a cache memory associated with an Owner processor;

updating a coherence directory for said memory block in said Home processor to indicate the write operation on the copy of said memory block in said cache memory associated with the Owner processor;

displacing said copy of said memory block from said cache memory prior to completion of operations on said memory block;

transmitting a message to said Home processor relinquishing exclusive control of said memory block, while indicating that said Owner processor should still be deemed a sharer of said memory block.

14. (Original) The method of claim 13, wherein the copy of the memory block is requested using a Load Lock instruction from the Owner processor to the Home processor.

15. (Original) The method of claim 13, wherein the Load Lock instruction forms part of a Load Lock/Store Conditional instruction pair.

16. (Original) The method of claim 13, wherein the act of updating the coherence directory includes modifying a register to indicate that the Owner processor has an exclusive copy of the memory block.

17. (Original) The method of claim 13, wherein the act of displacing said copy of said memory block includes comparing the address of any displaced memory block with an address of any memory block for which an exclusive copy resides in the Owner processor.

18. (Original) The method of claim 17, wherein the act of transmitting a message includes assertion of a Victim To Shared message if the address of the displaced memory block matches the address of any memory block for which an exclusive copy resides in the Owner processor, and wherein the directory associated with the Home processor indicates that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message.

19. (Original) The method of claim 18, further comprising the act of updating the coherence directory to indicate that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message.

20. (Original) The method of claim 13, further comprising the act of asserting a request to again obtain an exclusive copy of said memory block.

21. (Original) The method of claim 20, wherein, in response to request to again obtain an exclusive copy of the memory block, the Home processor determines if the Owner processor is a sharer of the memory block, and if so, the Home processor sends an exclusive copy of the memory block to the Owner processor.

22. (Original) The method of claim 21, wherein the Home processor invalidates all other sharers when it sends an exclusive copy of the memory block to the Owner processor.

23. (Original) The method of claim 20, wherein, in response to request to again obtain an exclusive copy of the memory block, the Home processor directory determines if the Owner processor is a sharer of the memory block, and if not, the Home directory sends a Store Conditional Failure message to the Owner processor.

24. (Original) A distributed multiprocessing computer system, comprising:

a first processor that includes a memory block and a directory associated with said memory block that tracks the status of said memory block;

a second processor that includes a cache memory, and wherein said second processor is capable of requesting an exclusive copy of said memory block that is stored in said cache memory; and

wherein said second processor may displace the exclusive copy of said memory block prior to completing processing of said memory block, and said second processor transmits a signal to said first processor indicating that said second processor relinquishes exclusive control of said memory block but should remain a sharer of said memory block.

25. (Original) The distributed multiprocessing computer system of claim 24, wherein said second processor obtains an exclusive copy of said memory block by issuing a Load Lock instruction, and wherein the directory associated with the first processor indicates that said second processor has obtained exclusive control of said memory block.

26. (Original) The distributed multiprocessing computer system of claim 24, wherein said second processor is capable of executing multiple threads concurrently, and may displace data associated with a non-executing thread from its associated cache memory.

27. (Original) The distributed multiprocessing computer system of claim 24, wherein said second processor includes a register in which an address is stored

representing the memory block exclusively obtained from said first processor, and wherein said second processor compares the address of any displaced data with the address stored in said register.

28. (Original) The distributed multiprocessing computer system of claim 27, wherein the second processor asserts a Victim To Shared message if the address of any displaced data matches the address stored in said register.

29. (Original) The distributed multiprocessing computer system of claim 28, wherein the directory associated with the first processor indicates that said second processor has become a sharer of said memory block in response to said Victim To Shared message.

30. (Original) The distributed multiprocessing computer system of claim 24, wherein said second processor subsequently re-obtains an exclusive copy of said memory block from said first processor to complete processing of said memory block.

31. (Original) The distributed multiprocessing computer system of claim 30, wherein the second processor asserts a request to read, modify, and conditionally store said memory block to said first processor.

32. (Original) The distributed multiprocessing computer system of claim 31, wherein, in response to the request to read, modify, and conditionally store said memory block, the first processor determines if the second processor is a sharer of the memory block, and if so, the first processor sends an exclusive copy of the memory block to the second processor.

33. (Original) The distributed multiprocessing computer system of claim 32, wherein the first processor invalidates all other copies of said memory block when it sends an exclusive copy of the memory block to the second processor.

34. (Original) The distributed multiprocessing computer system of claim 31, wherein, in response to the request to read, modify, and conditionally store said memory block, the first processor determines if the second processor is a sharer of the memory block, and if not, the first processor sends a failure message to the second processor.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.